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PATENT

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: William A. Harris
Examiner: Cox, Cassandra

Serial No.: 09/751,610
Group Art Unit: 2816

Filed: December 29, 2000
Docket: H16-26054 (256.058US1)

Title: PRECISION PHASE GENERATOR

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PATENT & TRADEMARK OFFICE

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

Applicant has reviewed the Office Action mailed on November 27, 2001. Please amend the above-identified patent application as follows.

IN THE DRAWINGS

The drawings are objected to because in Figure 2 there is no connection between output 217 and the clock input (CLK) of flip-flop 220. Correction is required.

Enclosed is a copy of Figure 2 of the drawings showing a proposed amendment to Figure 2 in red ink showing that output 217 and the clock input (CLK) are connected. The proposed change is clearly supported by the written specification (page 5, lines 13-28) since connecting the clock signal to each stage, including stage 220 of the Johnson counter is inherent to operation of the counter as described.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect cancellation of claims 10 and 18, amendment of previously pending claims 1, 6, 7, 13, 16 and 20, and addition of no new claims. The specific amendments to individual claims are detailed in the following marked up set of claims.

1. (Amended) A circuit for dividing an input clock signal into N clock signals having a relative phase separation of 360°/2N [clock signals], where N is a positive integer, the circuit comprising: